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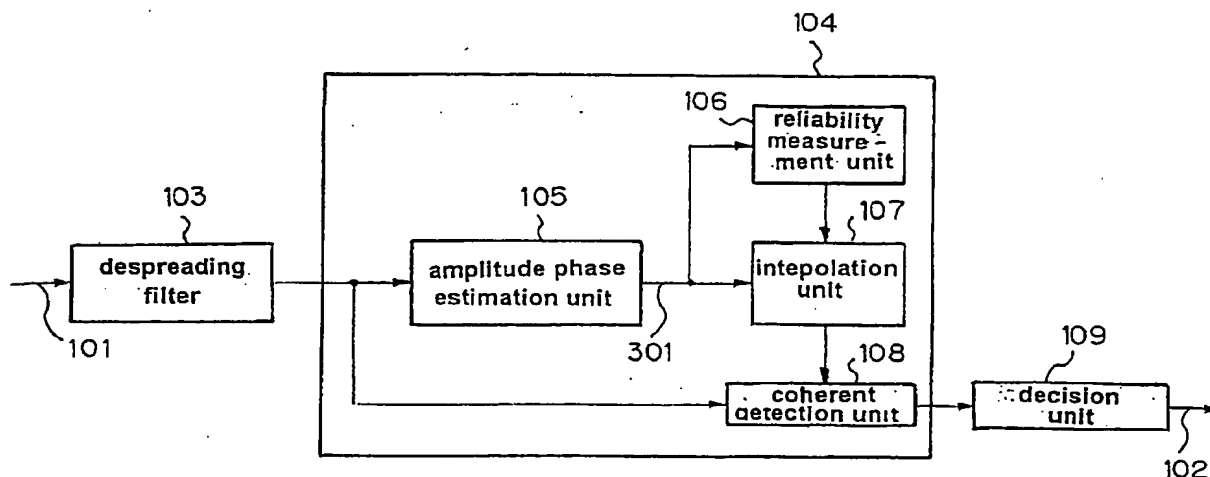
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(54) **Decode circuit for code division multiple access receiver**

(57) To improve the capacity of coherent detection of the spread spectrum (SS) signal, when interference and noise can not be neglected, an amplitude phase estimation unit outputs a transmission line estimation value including fluctuations in the transmission lines, using known pilot signals of which transmission sequences are known. The pilot signal is extracted from the de-

spread signal through despreading filter. A reliability measurement unit pursues a reliability value of transmission line estimation value. An interpolation unit generates vectors for compensating the phase, by deciding a method of interpolation on the basis of the reliability. A coherent detection unit compensates the amplitude and phase of information symbol to execute the coherent detection.

FIG.1



## Description

### BACKGROUND OF THE INVENTION

#### 1. Technical Field of the Invention

**[0001]** The present invention relates to a decoding circuit for receivers in mobile communication systems using code division multiple access (CDMA).

#### 2. Description of the Prior Art

**[0002]** Conventional transmitters for spread spectrum (SS) communication under the CDMA modulate communication data which are modulated beforehand by one of the modulation techniques. In other words, the modulated communication data are further modulated by Pseudo Noise (PN) sequence for SS modulation in order to widen the transmission bandwidth. The widened transmission bandwidth is used for a plurality of channels, wherein different PN sequences are assigned for every user or every kind of information.

**[0003]** Therefore, receivers firstly despread the wide-band SS signal into its original bandwidth and then decode, the despread signal by using conventional techniques. Here, a correlation of PN sequence is detected between the received signal and the receiver side by despread filter such as a matched filter which handles the PN sequence as tap coefficients, or an adaptive filter which optimizes the despreading process by varying the tap coefficients.

**[0004]** The receiving side can pick up a communication signal among multiplexed communication signals by detecting the correlation. The picked-up signal is a complete autocorrelation of the desired signal, when the PN sequence of the receiving side has no cross-correlation with other PN sequences. However, in general, PN sequences have cross-correlation with each other. Therefore, the output from the despread filter contains interference signals which are not desired by the receiving side. The above-mentioned interference signals increase with the number of communication channels and degraded the quality of received signal which is further degraded by thermal noise in the receiver and noises in transmission lines.

**[0005]** In the CDMA transmission, wherein an information signal is spread by PN signal of which the speed is higher than that of the information signal, prescribed pilot signals are inserted periodically in between the information signals, as shown in Figure 8. Therefore, phase vectors of the information symbols are obtained by an interpolation on the basis of phase vectors of the pilot symbols, as shown in Figure 9. Here, phase vector 1001 shows a track of the end point of every symbol due to fluctuations in the transmission lines. Phase vector 1002 is a phase vector of every information symbol obtained by interpolation. Phase vector 1003 is a phase vector which is an average phase vector in pilot symbol

periods.

**[0006]** A decode circuit implementing the above-mentioned method is shown in Figure 10. The decode circuit as shown in Figure 10 comprises matched filter 803 which operates under chip cycle  $T_c$  with a tap length of 1 symbol, interpolation detection unit 807, and Decision unit 109.

**[0007]** The decode circuit as shown in Figure 10 despreads SS signal 101, executes coherent detection, and outputs identified signal 102 on the basis of coherent detection.

**[0008]** Matched filter 803 comprises a plurality of delay units 804, a plurality of tap coefficient multipliers 805, and tap signal adder 806. Further, interpolation synchronous detector 807 for compensating a phase difference from matched filter 803 comprises amplitude phase estimation unit 105, first order interpolation unit 809, and coherent detection unit 108.

**[0009]** Amplitude phase estimation unit 105 pursues transmission estimation value 301 concerning the amplitude and phase in the transmission line, on the basis of a received phase of the pilot signal contained in the despread signal from matched filter 806.

**[0010]** First order interpolation unit 809 interpolates a received phase vector, inspecting a location of each information symbol.

**[0011]** Coherent detection unit 108 executes coherent detection, by compensating errors in the amplitude and phase of the information symbol on the basis of the received phase vector which is obtained by first order interpolation unit 809.

**[0012]** Decision unit 109 identifies the phase of the output from interpolation coherent detection unit 807. The output from Decision unit 109 is Identified signal 102.

**[0013]** SS signal 101 as shown in Figure 10 which contains known pilot symbol is inputted into matched filter 803 which has "M" taps extracted every chip cycle  $T_c$ . Here, an integer "M" is a spread factor. Signal vectors of each tap inputted into matched filter 803 are multiplied by tap coefficient vectors of which coefficient is determined by PN sequence. The tap coefficient vector is  $C_M, C_{M-1}, \dots, C_2, C_1$ , as shown in Figure 10. Then, the signals from each tap are added in tap signal adder 806 and outputted as a despread signal. Then, amplitude phase estimation unit 105 in interpolation coherent detection unit 807 pursues, by using the known pilot symbol, a received phase vector which represents errors in amplitude and phase due to the fluctuation of transmission lines. First order interpolation unit 809 interpolates a received phase vector, inspecting a location of each information symbol. Coherent detection unit 108 executes coherent detection, by compensating errors in the amplitude and phase of the information symbol on the basis of the received phase vector which is obtained by first order interpolation unit 809. Decision unit 109 identifies the phase of the output from interpolation coherent detection unit 807. The output from Decision unit 109 is

Identified signal 102.

[0014] The conventional decode circuit as shown in Figure 10 compensates fading distortion by using the pilot signal.

[0015] However, when received SS signal contains the interference and noise which can not be neglected, the pilot signal is also distorted. Therefore, the coherent detection is not correctly executed, because the transmission lines can not be estimated correctly.

[0016] Therefore, the conventional decode circuit has a disadvantage in that the coherent detection is not correctly executed, when the interference and noise can not be neglected

## SUMMARY OF THE INVENTION

[0017] Therefore, an object of the present invention is to provide a decode circuit with improved capability of coherent detection such that transmission lines are estimated correctly, even when the received SS signal contains much interference and noise.

[0018] A decode circuit of the present invention comprises a despreading filter for despreading spread spectrum (SS) signal, an amplitude phase estimation unit which estimates the amplitude and phase in transmission lines on the basis of pilot signals included in the despread signal, a reliability measurement unit for calculating a reliability value of the estimated amplitude and phase in the transmission lines, an interpolation unit for compensating the phase of information symbols by deciding a method of interpolation on the basis of the reliability, a coherent detection unit which detects the despread signal by using the interpolated estimation value in the transmission lines, and a decision unit for identifying the output from the coherent detection unit on the basis of its phase.

[0019] In short, the decode circuit of the present invention measures the reliability of the transmission line estimation value. Further, an interpolation method is decided on the basis of the reliability. Then, compensation vectors for compensating the phase are generated by the decided interpolation method to execute the coherent detection.

[0020] Therefore, the coherent detection is executed exactly, even when the interference and noise cannot be neglected.

[0021] Here, the reliability measurement unit may also calculate a reliability value of the detected signal outputted from the coherent detection unit.

[0022] According to the decode circuit of the coherent detection of the spread spectrum (SS) signal is optimized, even when the interference and noise can not be neglected.

## BRIEF EXPLANATION OF THE DRAWINGS

[0023] Figure 1 is a block diagram of a decode circuit of the first mode of embodiment of the present invention.

[0024] Figure 2 is an illustration for explaining an optimum interpolation by using pilot symbols.

[0025] Figure 3 is a block diagram of reliability measurement unit 106 and interpolation unit 107 as shown in Figure 1.

[0026] Figure 4 is a block diagram of a decode circuit of the second mode of embodiment of the present invention.

[0027] Figure 5 is a block diagram of reliability measurement unit 408 as shown in Figure 4.

[0028] Figure 6 is a block diagram of reliability measurement unit 408a in a decode circuit of the third mode of embodiment of the present invention.

[0029] Figure 7 is a block diagram of reliability measurement unit 408b in a decode circuit of the fourth mode of embodiment of the present invention.

[0030] Figure 8 is an illustration for explaining a signal frame structure including pilot symbols.

[0031] Figure 9 is an illustration for explaining a first order interpolation using the pilot symbol.

[0032] Figure 10 is a block diagram of a conventional decode circuit for spread spectrum (SS) signals.

## PREFERRED EMBODIMENT OF THE INVENTION

[0033] The mode of embodiment of the present invention is explained, referring to the drawings.

### (First Mode of Embodiment)

[0034] A block diagram of a decode circuit of the first mode of embodiment of the present invention is shown in Figure 1. Reference numbers are commonly used in Figures 1 and 10.

[0035] The decode circuit as shown in Figure 1 comprises despreading filter 103, interpolation coherent detection unit 104, and Decision unit 109. Matched filter 803 as shown in Figure 10 is an example of despreading filter 103.

[0036] Further, interpolation coherent detection unit 104 for compensating the amplitude and phase from despread filter 103 comprises amplitude phase estimation unit 105, reliability measurement unit 106, interpolation unit 107, and coherent detection unit 108.

[0037] SS signal 101 as shown in Figure 1 which contains known pilot symbols periodically is despread by despreading filter 103 and an SS signal in a certain channel is outputted. Then, interpolation coherent detection unit 104 estimates transmission line estimation value 301 concerning characteristics of the amplitude and phase of the transmission line by using amplitude phase estimation unit 105.

[0038] Further, reliability measurement unit 106 calculates the reliability of transmission line estimation value 301. Interpolation unit 107 decides an interpolation method on the basis of the calculated reliability, and interpolates transmission line estimation value 301 on the basis of positions of information symbols. For example,

the transmission characteristics are estimated, taking into consideration transmission line estimation value 301 which is obtained in adjacent symbol intervals as shown in Figure 9, when the calculated reliability is greater than a prescribed threshold. In this case, estimation errors are considered to be small. On the other hand, when the calculated reliability is smaller than a prescribed threshold, the transmission characteristics are estimated, without taking into consideration transmission line estimation value 301, as shown in Figure 2.

[0039] In Figure 2, received phase vector 1004 indicates average received phase vector averaged over the pilot symbol period after 2 slots. Received phase vector 1005 indicates average received phase vector averaged over the pilot symbol period after 1 slot. Received phase vector 1006 indicates interpolated received phase vector. Received phase vector 1007 indicates average received phase vector averaged over the present symbol period. Here, received phase vector 1007 can not be employed for interpolation, due to its low reliability.

[0040] Then, coherent detection unit 108 executes coherent detection in interpolation unit 107 on the basis of transmission line estimation value interpolated for every information symbol. Decision unit 109 determines the phase of the output signal from interpolation coherent detection unit 104 and outputs the above-mentioned output signal from interpolation coherent detection unit 104 as an identified signal 102.

[0041] Despreading filter 103, amplitude phase estimation unit 105, coherent detection unit 108, and decision unit 109 are similar to the corresponding elements as shown in Figure 10. Therefore, only reliability measurement unit 106 and interpolation unit 107 are further explained concretely, referring to Figure 3.

[0042] As shown in Figure 3, reliability measurement unit 106 comprises power calculation unit 303, threshold supply unit 304, and reliability generation unit 305. Interpolation unit 107 comprises interpolation method instruction unit 306, first order interpolation unit 307, and second interpolation unit 308.

[0043] Power calculation unit 303 calculates the power of transmission line estimation value 301 by squaring the amplitude of transmission line estimation value 301.

[0044] Threshold supply unit 304 supplies reliability generation unit 305 with a prescribed threshold.

[0045] Reliability generation unit 305 pursues the reliability of transmission line estimation value 301, by comparing the threshold from threshold supply unit 304 with the power from power calculation unit 303. Concretely, reliability is set to be "1", when the power is greater than the threshold, because the reliability is high in this case, while reliability is set to be "0", when the power is smaller than the threshold, because the reliability is low in this case. The reliability is sent to interpolation method instruction unit 306.

[0046] Interpolation method instruction unit 306 transfers transmission line estimation value 301 to first order

interpolation unit 307, when the reliability is "1", while it transfers transmission line estimation value 301 to second order interpolation unit 308, when the reliability is "0".

[0047] First order interpolation unit 307 interpolates the transmission line estimation value estimated in the adjacent pilot symbol periods into each information symbol, as shown in Figure 9.

[0048] Second order interpolation unit 308 interpolates the transmission line estimation value estimated in four pilot symbol periods into each information symbol, as shown in Figure 2, neglecting the transmission line estimation value of which the power is small. Here, the four pilot symbol periods are two periods before the present period and two periods after the present periods.

[0049] Next, the operation of the first mode of embodiment of the present invention is explained, referring to the drawings.

[0050] As shown in Figure 3, power calculation unit 303 inputs transmission line estimation value 301 and calculates a power of transmission line estimation value 301 by squaring the amplitude of transmission line estimation value 301. Then, reliability generation unit 305 pursues the reliability value, by comparing the threshold from threshold supply unit 304 with the power of transmission line estimation value 301.

[0051] Interpolation method instruction unit 306 transfers transmission line estimation value 301 to first order interpolation unit 307, when the reliability is "1". First order interpolation unit 307 interpolates the transmission line estimation value estimated in the adjacent pilot symbol periods into each information symbol, as shown in Figure 9. Here, the adjacent pilot symbol periods are a period before the present period and a period after the present period.

[0052] On the contrary, interpolation method instruction unit 306 transfers transmission line estimation value 301 to second order interpolation unit 308, when the reliability is "0". Second order interpolation unit 308 interpolates the transmission line estimation value estimated in four pilot symbol periods into each information symbol, as shown in Figure 2, neglecting the transmission line estimation value of which power is small. Here, the four pilot symbol periods are two periods before the present period and two periods after the present periods.

[0053] As shown in Figure 2, three values among four transmission estimation values are employed for the second order interpolation, neglecting one of the estimation value of which power is small. Zero order interpolation, and weighted interpolation may be also employed. Further, higher order interpolation may be employed, using four or more estimation values.

[0054] Not only power itself but also a variance of power may be employed in the interpolation. In this case, the method as Figure 9 is employed for a small variance, while the method as set forth in Figure 2 is

employed for a great variance.

[0055] Furthermore, a plurality of thresholds may be introduced, or the threshold may be varied adaptively.

#### (Second Mode of Embodiment)

[0056] A block diagram of the decode circuit of the second mode of embodiment of the present invention is shown in Figure 4. Reference numbers are commonly used in Figures 1 and 4.

[0057] The decode circuit as shown in Figure 4 comprises despreading filter 103, interpolation coherent detection unit 404, reliability measurement unit 408, rake combining unit 409, and decision unit 109.

[0058] Further, interpolation coherent detection unit 404 for compensating the phase of the signal outputted from despreading filter 103 comprises transmission line amplitude phase estimation unit 105, interpolation unit 107, and coherent detection unit 108.

[0059] Comparing with the first mode of embodiment as shown in Figure 1, the decode circuit of the second mode of embodiment has reliability measurement unit 408 outside interpolation coherent detection unit 404, while reliability measurement unit 106 is provided inside interpolation coherent detection unit 104. Further, rake combining unit 409 is added.

[0060] Reliability measurement unit 408 measures the reliability of a signal detected by coherent detection unit 108. Rake combining unit 409 combines a plurality of detected signals. The operation of rake combining unit 409 is well known.

[0061] Figure 5 is a block diagram of reliability measurement unit 408 as shown in Figure 4.

[0062] Input terminal 501 of reliability measurement unit 408 accepts the signal detected by coherent detection unit 108. Input terminal 502 accepts the output from rake combining unit 412 which combines signals from a plurality of paths. Further, input terminal 503 outputs the reliability value.

[0063] Reliability measurement unit 408 comprises SIR (signal to interference ratio) calculation unit 504, threshold supply unit 505, and reliability generation unit 506.

[0064] SIR calculation unit 504 calculates SIR of the signal which is processed by coherent detection unit 108. SIR may be calculated, for example, by inversely modulating the detected signal by a known sequence which makes up a known pilot symbol. In this case, the SIR is defined as a ratio of the squared value of the average of the above-mentioned inversely modulated signal to the variance of the above-mentioned signal.

[0065] Reliability generation unit 506 pursues the reliability value, by comparing the threshold from threshold supply unit 505 with the SIR value. Concretely, reliability is set to be "1", when the SIR is greater than the threshold, because the reliability is high in this case, while reliability is set to be "0", when the SIR is smaller than the threshold, because the reliability is low in this

case.

#### (Third Mode of embodiment)

5 [0066] In the third mode of embodiment, reliability measurement unit 408 as shown in Figure 4 of the second mode of embodiment is replaced by reliability measurement unit 408a as shown in Figure 6.

10 [0067] Reliability measurement unit 408a comprises decision unit 601, error rate calculation unit 602, threshold supply unit 505, and reliability generation unit 506.

[0068] Decision unit 601 executes determination and identification of the detected signal from interpolation coherent detection unit 108 through input terminal 501. Error rate calculation unit 602 calculates an error rate of the identified signal, by using a part of the identified signal of which transmission sequence is known. Then, reliability generation unit 506 pursues the reliability value, by comparing the threshold from threshold supply unit 505 with the error rate. Concretely, reliability is set to be "1", when the error rate is smaller than the threshold, because the reliability is high in this case, while reliability is set to be "0", when the error rate is greater than the threshold, because the reliability is low in this case.

#### (Fourth Mode of embodiment)

[0069] In the fourth mode of embodiment, reliability measurement unit 408 as shown in Figure 4 of the second mode of embodiment is replaced by reliability measurement unit 408b as shown in Figure 7.

[0070] Error rate is measured by using a whole block of the identified signal in the fourth mode of embodiment, although only a part of the identified signal is used in the third mode of embodiment.

[0071] Reliability measurement unit 408b comprises Decision units 601 and 701, error rate calculation unit 703, threshold supply unit 505, and reliability generation unit 506. Decision units 601 and 701, threshold supply unit 505, and reliability generation unit 506 are similar to those as shown in Figure 6.

[0072] Decision unit 702 executes determination and identification of the detected signal from rake combining unit 409 through input terminal 502.

45 [0073] Error rate calculation unit 703 calculates the error rate of the detected data, on the basis of the outputs from Decision units 601 and 702. Here, the input of Decision units 601 is a signal detected by interpolation coherent detection unit 108, while the input of Decision units 702 is the output of rake combining unit 409. Then, reliability measurement unit 506 pursues the reliability value, by comparing the threshold from threshold supply unit 505 with the error rate.

55 [0074] Although the present invention has been shown and described with respect to the best mode embodiment thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions, and additions in the form and detail

thereof may be made therein without departing from the spirit and scope of the present invention.

[0075] For example, rake combining unit in the first to fourth modes of invention may be replaced by diversity combining unit, de-interleave unit, error correction unit. Further, interpolation may be executed on the basis of an error rate of a pilot symbol of which the transmission sequence is known, or a check bit inserted into a frame, by using a rake combined signal only.

## Claims

1. A decode circuit for decoding spread spectrum signal including pilot signal, which comprises:
  - a despreading filter for despreading said spread spectrum (SS) signal;
  - an amplitude phase estimation unit which estimates the amplitude and phase on the basis of said pilot signal;
  - a reliability measurement unit for calculating the reliability of an output of said amplitude phase estimation unit;
  - an interpolation unit for compensating the phase of an information symbol included in the output of said amplitude phase estimation unit;
  - a coherent detection unit which executes coherent detection on the basis of the output from said interpolation unit and the output from said despreading filter; and
  - a decision unit for identifying the output from coherent detection unit on the basis of the phase of the output signal from said coherent detection unit.
2. The decode circuit according to Claim 1, wherein said reliability measurement unit comprises:
  - a power calculation unit for calculating the power on the basis of the output from said amplitude phase estimation unit;
  - a threshold supply unit for supplying one or more prescribed thresholds; and
  - a reliability generation unit for calculating the reliability of the output of said amplitude phase estimation unit, by comparing said prescribed thresholds with the output from said power calculation unit;
 wherein said reliability is set to be "1", when said output from said power calculation unit is greater than said prescribed thresholds, while said reliability is set to be "0", when said output from said power calculation unit is smaller than said prescribed thresholds.
3. The decode circuit according to Claim 1, wherein said interpolation coherent detection unit comprises:
  - a first order interpolation unit for interpolating the estimated output from said amplitude phase estimation unit which is estimated on the basis of the adjacent two pilot symbols before and after an information symbol;
  - a second order interpolation unit for interpolating the output from said amplitude phase estimation unit which is estimated on the basis of the adjacent two pilot symbols before said information symbol and the adjacent two pilot symbols after said information symbol; and
  - an interpolation method instruction unit for transferring said output from said amplitude phase estimation unit to said first order interpolation unit, when said reliability is "1", and for transferring said output from said amplitude phase estimation unit to said second order interpolation unit, when said reliability is "0".
4. A decode circuit for decoding spread spectrum signal including pilot signal, which comprises:
  - a despreading filter for despreading said spread spectrum (SS) signal;
  - an amplitude phase estimation unit which estimates the amplitude and phase on the basis of said pilot signal;
  - an interpolation unit for compensating the phase of information symbol included in the output of said amplitude phase estimation unit;
  - a coherent detection unit which executes coherent detection on the basis of the output from said interpolation unit and the output from said despreading filter;
  - a reliability measurement unit for calculating reliability of the output of said coherent detection unit; and
  - a decision unit for identifying the output from coherent detection unit on the basis of the phase of the output signal from said coherent detection unit.
5. The decode circuit according to Claim 4, wherein said reliability measurement unit comprises:
  - a signal to interference ratio (SIR) calculation unit for calculating the SIR of the output from said coherent detection unit;
  - a threshold supply unit for supplying one or more prescribed thresholds; and
  - a reliability generation unit for calculating said reliability, by comparing said prescribed thresholds with said SIR, wherein said reliability is set to be "1", when said SIR is greater than said prescribed thresholds, while said reliability is set to be "0", when said SIR is smaller than said

prescribed thresholds.

6. The decode circuit according to Claim 4, wherein said reliability measurement unit comprises:

an error rate calculating unit for calculating the error rate of the output from said decision unit; a threshold supply unit for supplying one or more prescribed thresholds; and a reliability generation unit for calculating said reliability, by comparing said prescribed thresholds with said error rate, wherein said reliability is set to be "1", when said error rate is smaller than said prescribed thresholds, while said reliability is set to be "0", when said error rate is greater than said prescribed thresholds.

7. The decode circuit according to Claim 4, wherein said reliability measurement unit comprises;

another decision unit for identifying the output from said coherent detection unit, a rake combining unit for combining a plurality of detected signals; other decision unit for identifying the output from said rake combining unit; an error rate calculating unit for calculating the error rate on the basis of the output from said another decision unit and the output from said other decision unit; a threshold supply unit for supplying one or more prescribed thresholds; and a reliability generation unit for calculating said reliability, by comparing said prescribed thresholds with said error rate, wherein said reliability is set to be "1", when said error rate is smaller than said prescribed thresholds, while said reliability is set to be "0", when said error rate is greater than said prescribed thresholds.

8. The decode circuit according to Claim 4, wherein said interpolation coherent detection unit comprises:

a first order interpolation unit for interpolating the estimated output from said amplitude phase estimation unit which is estimated on the basis of the adjacent two pilot symbols before and after an information symbol; a second order interpolation unit for interpolating the output from said amplitude phase estimation unit which is estimated on the basis of the adjacent two pilot symbols before said information symbol and the adjacent two pilot symbols after said information symbol; and an interpolation method instruction unit for transferring said output from said amplitude phase estimation unit to said first order interpolation unit, when said reliability is "1", and for transferring said output from said amplitude phase estimation unit to said second order interpolation unit, when said reliability is "0".

lation unit, when said reliability is "1", and for transferring said output from said amplitude phase estimation unit to said second order interpolation unit, when said reliability is "0".

9. The decode circuit according to Claim 1, wherein said despreading filter is a matched filter.

10. The decode circuit according to Claim 4, wherein said despreading filter is a matched filter.

FIG.1

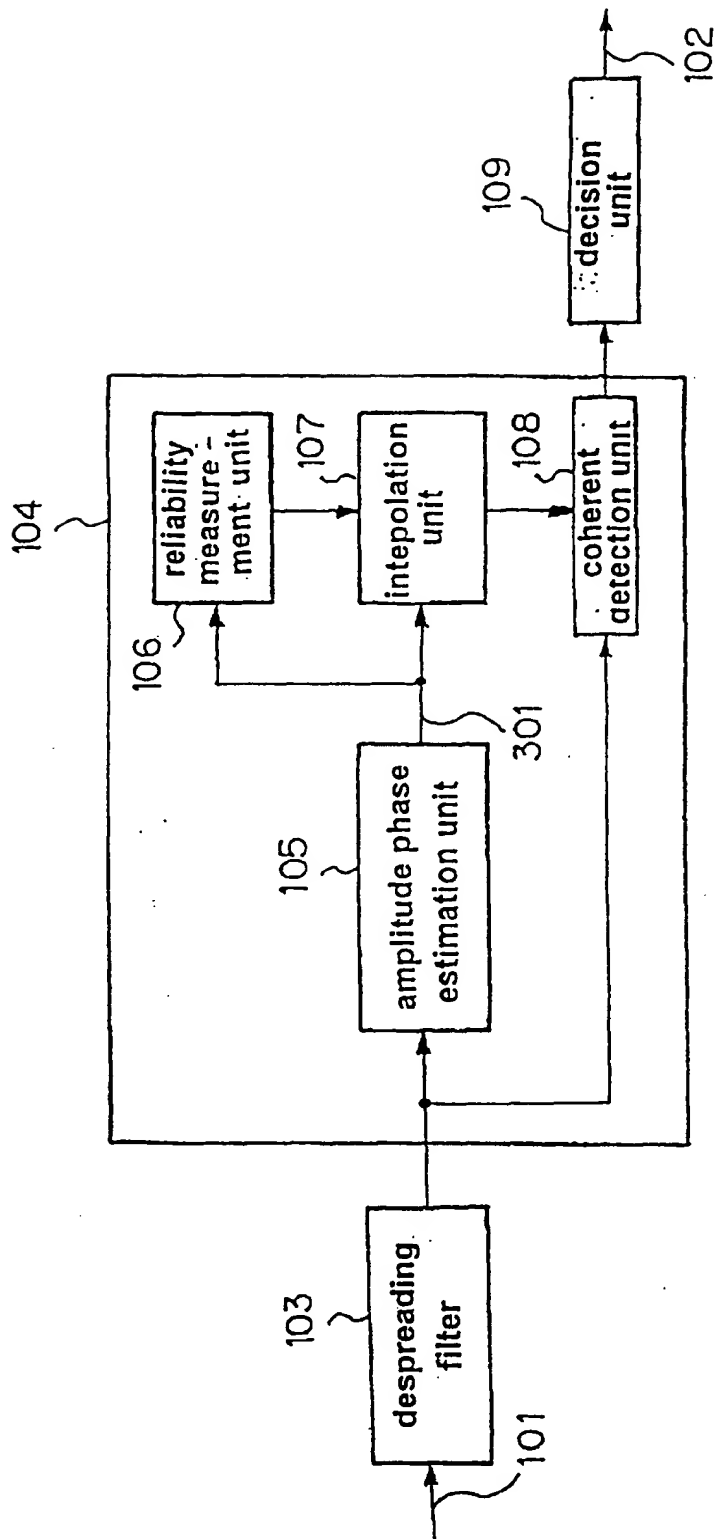




FIG.2

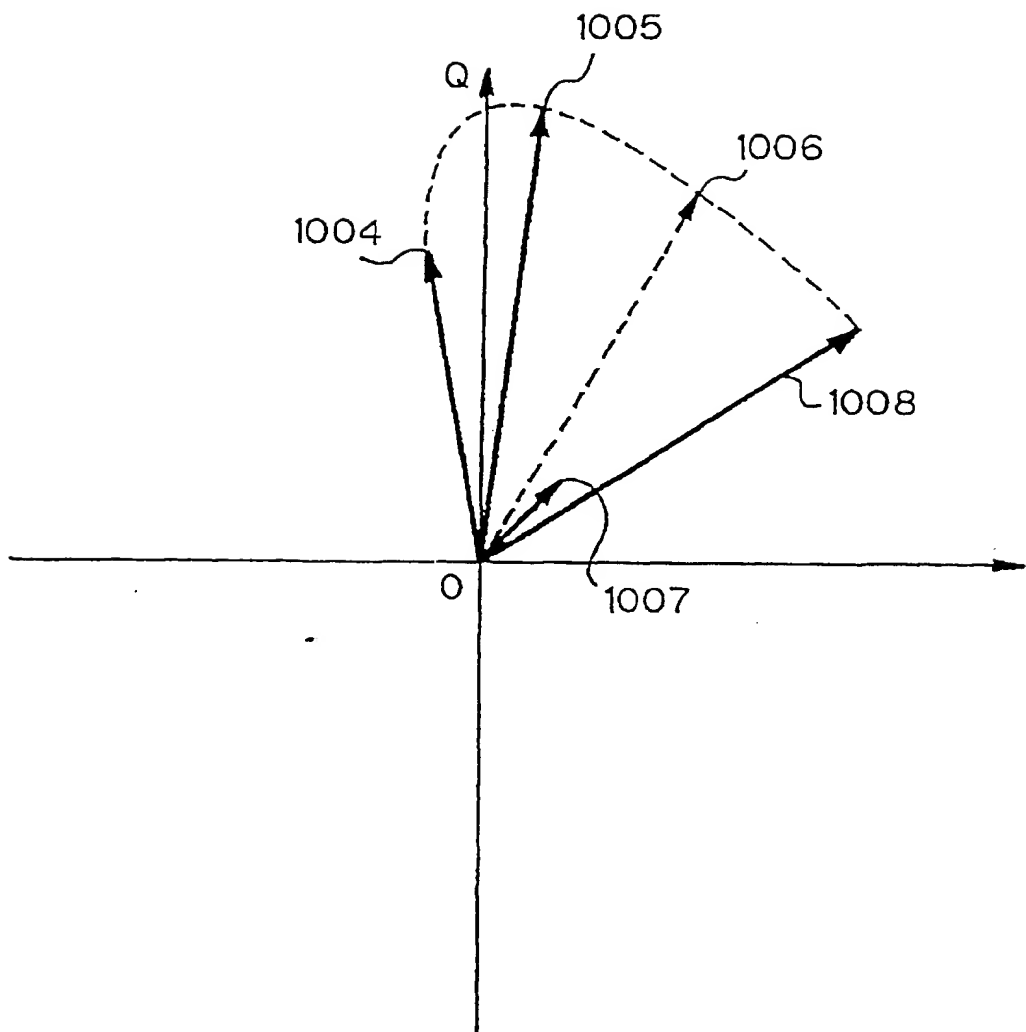


FIG.3

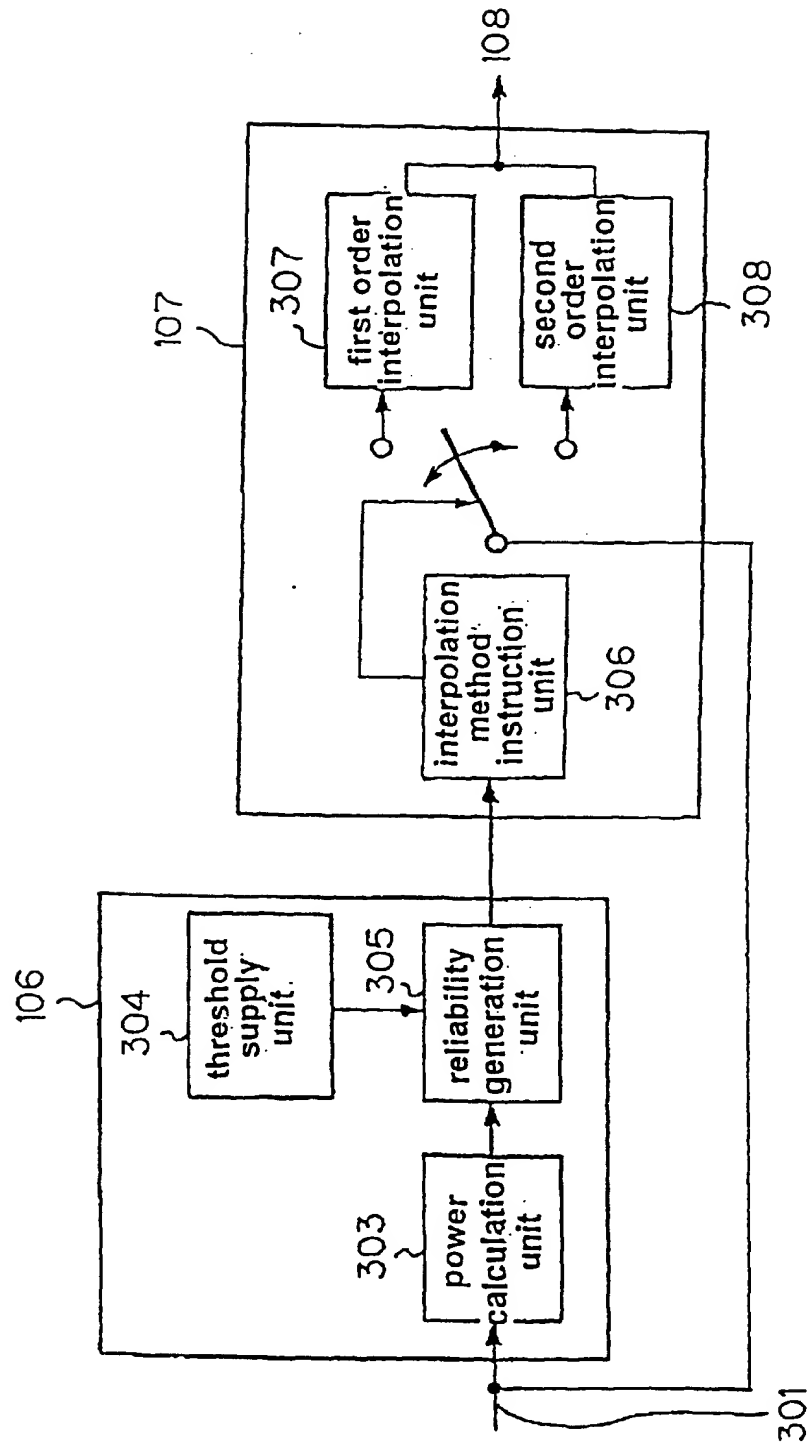


FIG.4

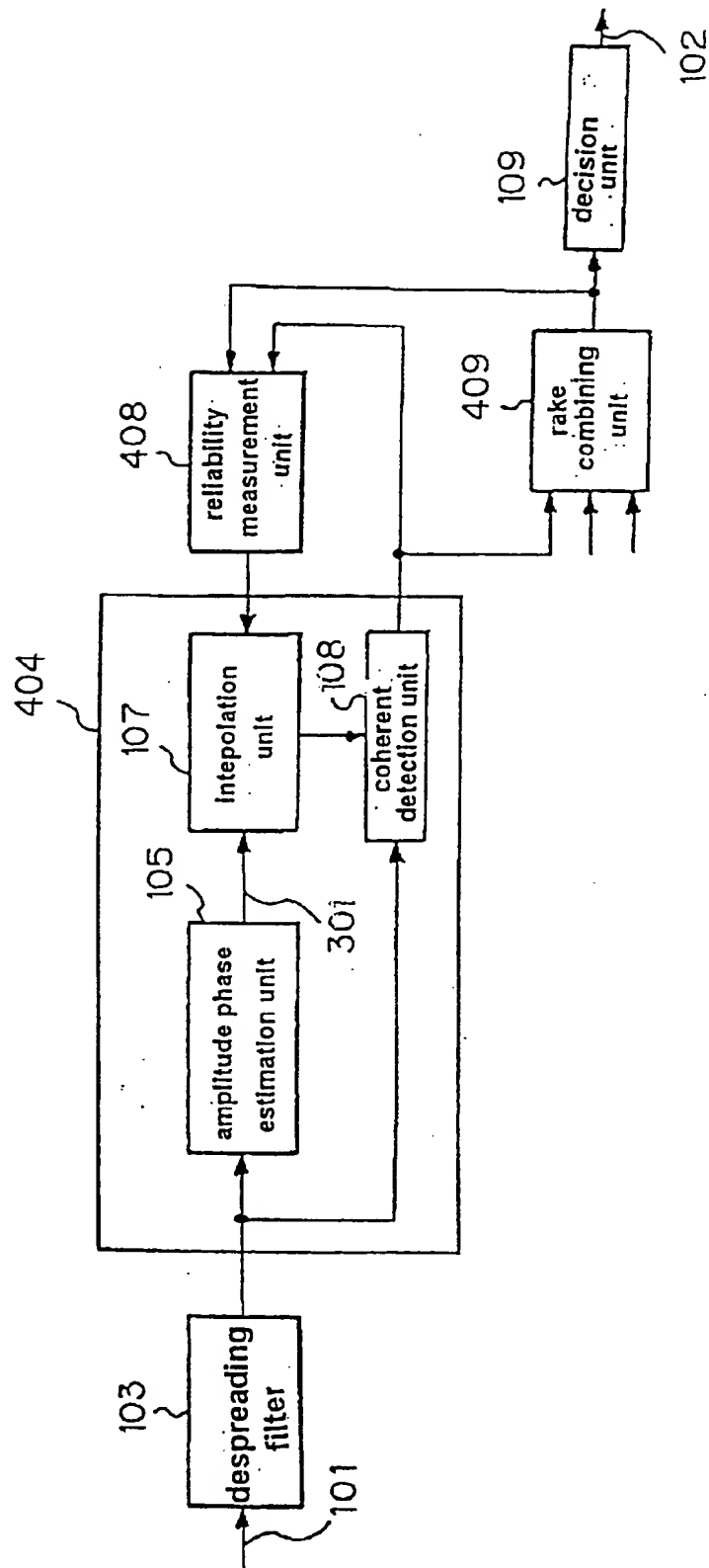


FIG.5

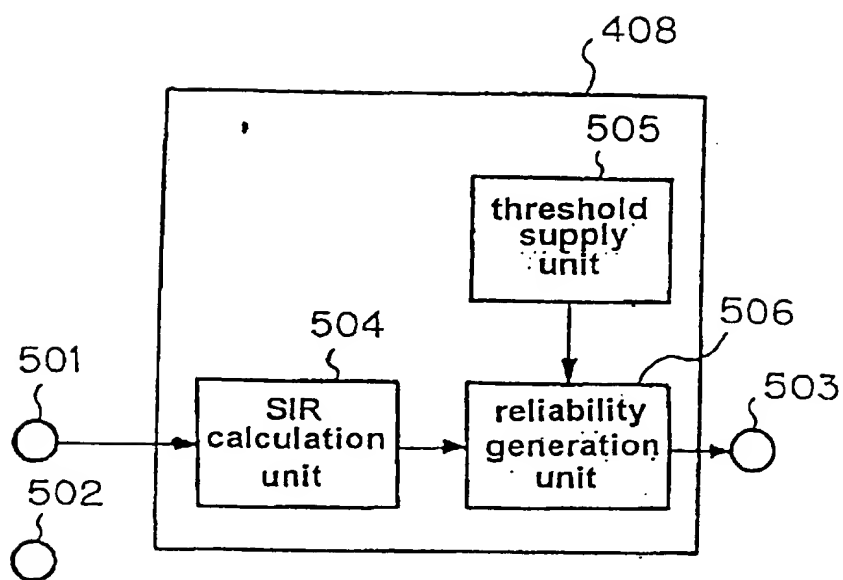


FIG.6

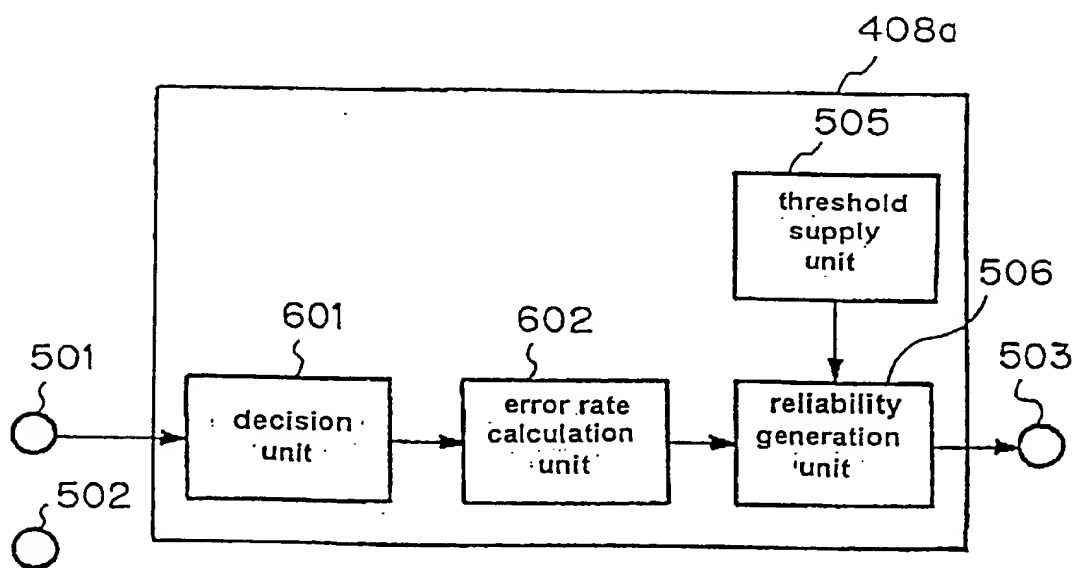


FIG.7

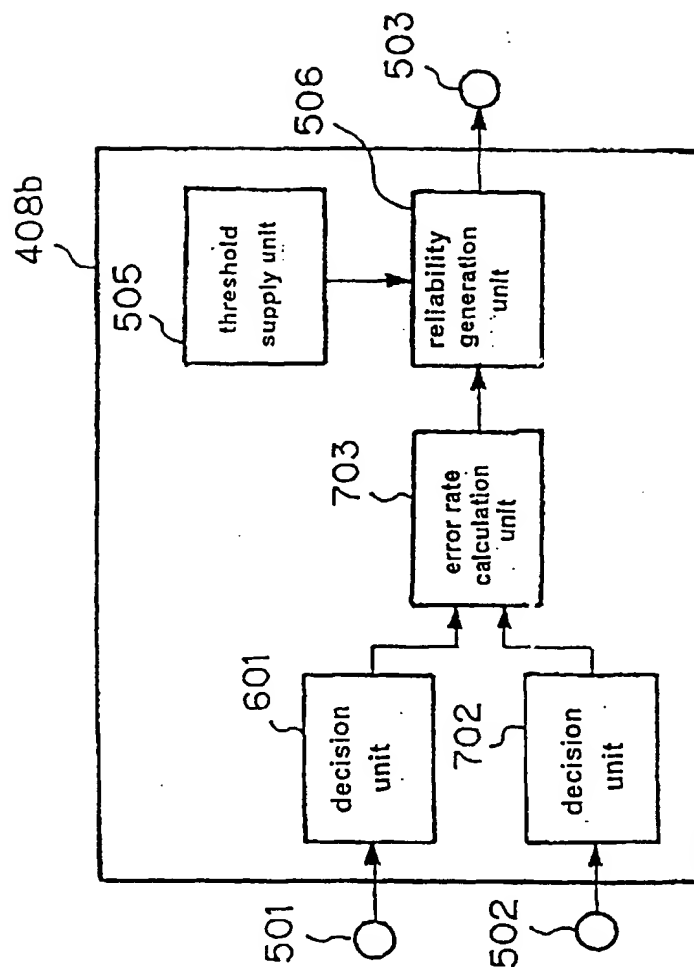


FIG.8

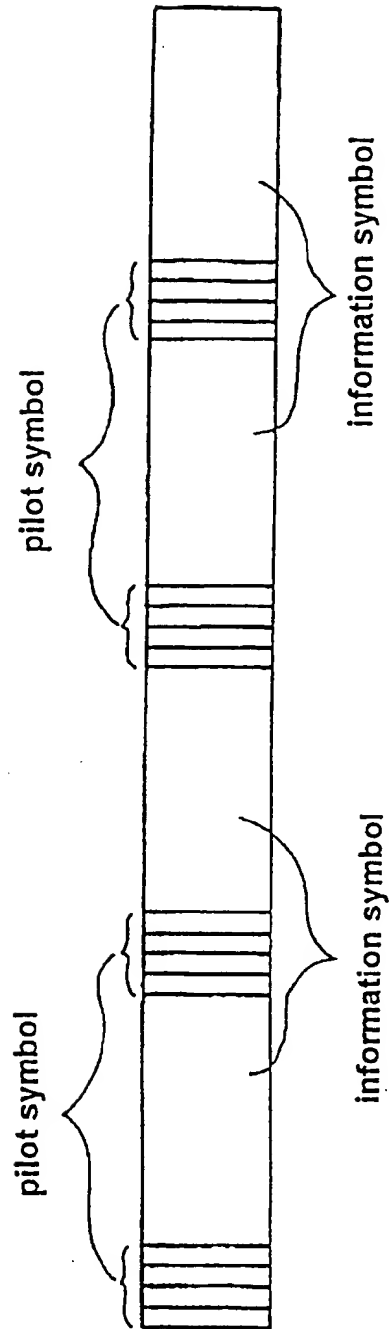


FIG.9

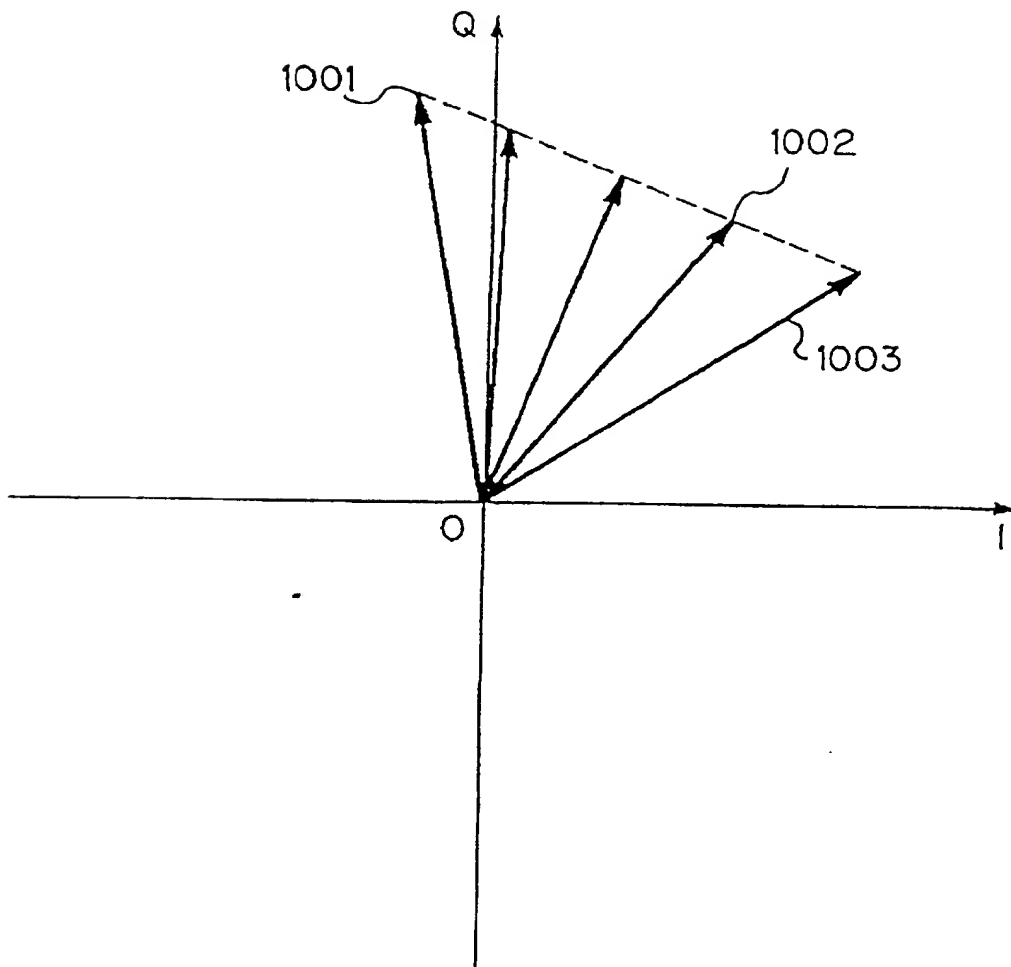


FIG.10

